What is claimed is:

Sub A1

1. An active pixel sensor device, comprising:

a pixel sensor array of photosensor elements, arranged in logical units, each photosensor element defining a pixel with a CMOS photosensor element, an in-pixel buffer element and an in-pixel selector element, said photosensor elements arranged in an array; and

a plurality of analog-to-digital converters, formed on the same substrate as said pixel sensor array, and each associated with at least two logical units of the pixel sensor array, each analog-to-digital converter including an ADC portion which receives an analog signal from one of said pixel sensors when said selector element is enabled, and converts said analog signal to a digital value, and at least two unit storage elements, associated with said analog to digital converter, each storing one unit of digital information indicating the output signal.

2. A sensor as in claim 1, wherein said logical units are lines of the array including either columns of the array or rows of the array.

3. A device as in claim 2, wherein said analog-to-digital converters are associated with at least two adjacent lines of the array.

4. A device as in claim 3, further comprising a readout controller, controlling readout of information from the photosensor elements, by controlling said analog-to-digital converters to each convert information from a first line of the array, to store said information from the first line of the array in one of said unit storage elements, then to read out a second line of the array, and store said information from said second line of the array in the other of said unit storage elements, and then to read out the information from all of said unit storage elements in a desired order.

Sub B2 cont'd

5. A method of operating a pixel sensor array, comprising:

obtaining a pixel sensor array of photosensitive elements, each having a photosensitive element in a pixel, a buffer in said pixel associated with said photosensitive element, and a selector transistor in said pixel which is enabled to allow a signal from said pixel to pass, and disabled to block the signal from passing;

connecting a plurality of said outputs of said selector transistors to one another, to form a plurality of logical units, each logical unit formed by a plurality of said output transistors which are connected to one another;

receiving, in a plurality of A/D converter units, a plurality of image information from a plurality of A/D converter units and A/D converting said information and logically storing said information in a first storage unit;

receiving information in said plurality of A/D converter units from a second logical unit, adjacent to said first logical unit, and A/D converting and logically storing said additional information; and

reading out said information from said A/D conversion unit in a different order than an order in which the information was converted.

6. A method as in claim 5, wherein said different order is in a serial order.

7. A method as in claim 5, wherein said units are linear units which are one of rows and columns, said first order skips lines between conversions, and second order is a complete order.